

BUILT IN SELF TEST METHOD AND CIRCUIT
FOR PARALLEL OPTICAL TRANSMITTERS

5 BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the field of testing parallel optical communication transmitters.

10 Background Information

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SUMMARY OF THE INVENTION

It is, therefore, a principle object of the this invention to provide a built-in self test method and circuit for parallel laser transmitters.

5 It is another object of the invention to provide a built-in self test method and circuit for parallel laser transmitters that solves the above-mentioned problems.

10 These and other objects of the present invention are accomplished by the built-in self test method and circuit for parallel laser transmitters that are disclosed herein.

15 Asynchronous crosstalk measurements are performed when a single channel input is provided by a single data generator and channels adjacent thereto are switching asynchronous to the single data generator. Crosstalk and noise problems may be measured qualitatively and quantitatively by using a BIST generator that generates a pseudo-random bit sequence on many channels as an on-chip noise source. Furthermore, while in BIST mode, any combination of channels may switch at a rate determined by a BIST input clock, or held quiet at a static 0 or 1 for a DC coupled product. This is advantageous while analyzing parameters that are sensitive to noise or crosstalk. Therefore, it is desired that the optical output of a channel responds to the electrical input of that channel, while other channels are running in BIST mode.

25 As a result, the complexity of testing is significantly

reduced in comparison with conventional testing methods, as described in the example above, because only one data generator and one clock source are used. In the alternative, to reduce complexity of testing, fewer, or even no, switches that are capable of switching data at the full data rate, for example coaxial switches, are used. The reduction, or absence, of switches thus reduces complexity of testing. It also gives greater test coverage with only one data generator allowing the user to choose which optical outputs will output BIST data or external asynchronous data.

To that end, the present invention includes a BIST generator that is incorporated into a parallel optical transmitter. The parallel optical transmitter includes N laser driver channels in addition to the aforementioned BIST generator.

An external clock source is applied to the differential inputs of Channel N of the parallel optical transmitter. The external clock inputs are buffered by Channel N and applied to the clock input of the BIST generator. Control signal inputs EBIST and SBIST are used to put the transmitter array in BIST mode.

The external data inputs are applied to the inputs of a data receiver and a signal detector. The signal detector determines if a signal with a valid common mode voltage level is present on the Tx inputs. The data receiver buffers the Tx

inputs, and the outputs of the data receiver are connected to a multiplexer input. The BIST generator outputs are applied to a buffer before being connected to the B inputs of the multiplexer. A logic block controls which of two multiplexer inputs is passed by the multiplexer to the inputs of a laser driver. The laser driver then converts the differential input to a single ended current to drive the laser. Thus, the signal detector is connected in parallel with the data receiver and the output of the signal detector is passed to the multiplexer.

The combinations of EBIST, SBIST and SIGDET determines if the input data or BIST data gets passed to the laser driver. In particular, in the "hard BIST" (EBIST) mode, BIST signals are transmitted along all of Channels 0-N. On the other hand, in the "soft BIST" (SBIST) mode, if the signal detector determines the presence of a valid signal, the logic block makes the determination, based on a predetermined logic table, as to whether BIST data or real data is passed through the multiplexer to the inputs of the laser driver of that channel.

As an example, the signal detector is a pull-down detector. In operation, as the signal detector receives external data inputs, if a first node falls below a second node, the signal detection output goes low, indicating that a valid signal is not present, although any polarity may be produced by inverting the comparator inputs. If the external

inputs are held low, a comparator of the signal detector indicates that a valid signal is not present.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Figure 1 shows an example embodiment of a parallel optical communication transmitter, including a BIST generator, according to the present invention.

10 Figure 2 shows an example of a channel in the example embodiment of a parallel optical communication transmitter shown in Fig. 1, according to an example embodiment of the present invention.

15 Figure 3 shows an example of common mode pull-down detector, as utilized in the example of Figure 1, according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

20 Before beginning a detailed description of the invention, it should be noted that, when appropriate, like reference numerals and characters may be used to designate identical, corresponding or similar components in differing figure drawings. Further, in the detailed description to follow, example embodiments and values may be given, although the present invention is not limited thereto.

25 Figure 1 shows a BIST generator **5** is incorporated into the parallel optical transmitter **100**, in accordance with an

example embodiment of the present invention. Parallel optical transmitter **100** includes N laser driver channels Channels 0- N (**CH0-CHN**) in addition to the aforementioned BIST generator **5**.

INS
a4
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An external clock source **1** may be applied to the inputs of Channel N **CHN**, during BIST mode operation. Otherwise, the Channel N inputs are data. EBIST **11** and SBIST **12** are control signal inputs used to select the type of data that is passed to the laser driver, choosing from BIST data and external data. OR gate **7** enables the BIST generator **5**. Thus, when EBIST and SBIST are 0, BIST generator **5** is disabled, as will be described further below regarding Logic Block **70** in Fig. 2.

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Figure 2 shows the contents of each channel in Figure 1. The external data inputs **20** are applied to the inputs of Data Receiver **50** and Signal Detector **40**. Signal Detector **40** determines if a signal with a valid common mode (average voltage) is present on the Tx inputs **20**. The Data Receiver **50** buffers the Tx inputs **20**, and the outputs **55** of Data Receiver are connected to multiplexer input A **85**. The BIST generator **5** of Figure 1 generates BIST inputs **30**, and the inputs **30** are buffered by the BIST Buffer **60**. BIST Buffer outputs **65** are connected to the multiplexer input B **86**. Logic block **70** controls which of inputs "A" **85** or "B" **86** is passed by multiplexer **80** to the inputs of Laser Driver **90**. Laser Driver **90** then converts the differential input to a single ended

current **95** to drive the laser. Figure 2 shows, as an example, how Signal Detector **40** is connected in parallel with the Data Receiver **50** and how the output **45** of Signal Detector **40** is passed to the Multiplexer **80**.

5 The combinations of EBIST, SBIST and SIGDET determines if the input data or BIST data gets passed to the laser driver. In particular, in the "hard BIST" (EBIST) mode, BIST signals are transmitted along all of Channels 0-N. On the other hand, in the "soft BIST" (SBIST) mode, if Signal Detector **40**
10 determines the presence of a valid signal on the Tx inputs, Logic Block **70** allows Multiplexer **80** to pass the external data to the laser driver **90**.

15 Figure 3 shows Signal Detector **40** of Figure 2 in greater detail. As an example, Signal Detector **40** is a pull-down detector. In operation, as Signal Detector **40** receives external data inputs **20**, if node **A** falls below node **B**, the output SIGDET goes low, indicating that a valid signal is not present, although any polarity may be produced by inverting the comparator inputs. If the average of the input voltages at
20 node A falls below the voltage at node B, the comparator **110** indicates that a valid signal is not present.

For example, if the receiver common mode is X volts, and the single ended amplitude of both inputs is Y volts, then the lowest voltage the incoming signal can reach is $X - 0.5Y$ volts.

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1	0	0	BIST
1	0	1	BIST
1	1	0	TX
1	1	1	BIST

5.

EBIST and SBIST are selected globally. SIGDET 45 in Figure 2 is the signal produced by the Signal Detector 40. SIGDET 45 is logic high if a signal with valid common mode is applied to the Tx inputs 20 in Figure 2. SIGDET 45 is low when a signal with non-valid common mode is applied to Tx inputs 20 such as connecting them to ground in the case where PECL logic is used. EBIST forces the laser driver output 95 to be the BIST signal independent of the logic states of SBIST and SIGDET.

This concludes the description of the example embodiments. Although the present invention has been described with reference to illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope and spirit of the principals of the invention. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without department from the spirit of the

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